ABSTRACT OF THE DISCLOSURE

There is provided an error rate select circuit activated in an information sustaining mode, wherein a plurality of pieces of data is read out from a memory circuit comprising dynamic memory cells and inspection bits for detection and correction of an error existing in the pieces of data are generated. The inspection bits are stored in an additional memory circuit. An ECC circuit reads out the pieces of data from the memory circuit and the inspection bits associated with the pieces of data from the additional memory circuit to detect and correct an error existing in the pieces of data at fixed refresh intervals. If no error is detected, a first detection signal is accumulated in a first direction, that is, the first detection signal is added to a sum. If an error is detected, on the other hand, a second detection signal is accumulated in a second direction, that is, the second direction signal is multiplied by a weight to give a product before subtracting the product from the sum wherein the weight is large enough to result in a value of the product greater than the first detection signal. If the sum increases in the first direction, exceeding a predetermined value, the refresh period is lengthened by a predetermined incremental time. If the sum decreases in the second direction, becoming smaller than another predetermined value, on the other hand, the

refresh period is shortened by a predetermined decremental time.